

## CLAIMS

1 1. A method for generating a Cyclic Redundancy Check (CRC) in a system comprising the  
2 steps of:  
3 creating a circuit comprising a plurality of registers wherein each of the plurality of  
4 registers is associated with a corresponding logic gate; and  
5 programming a subset of the plurality of registers to have a value of zero and  
6 programming a corresponding subset of the logic gates to have a value of zero,  
7 wherein the step of programming is based on a pre-selected polynomial key word.

1 2. The method as recited in Claim 1, wherein the step of programming comprises:  
2 programming a first set of selection inputs, wherein:  
3 the step of programming the first set of selection inputs is based on the pre-  
4 selected polynomial key word;  
5 the first set of selection inputs is associated with:  
6 selecting corresponding input from each of the logic gates; and  
7 a shift logic that is associated with the plurality of registers.

1 3. The method as recited in Claim 1, wherein the step of programming comprises:  
2 programming a second set of selection inputs, wherein:  
3 the second set of selection inputs is associated with selecting corresponding input  
4 to each of the logic gates;  
5 the second set of selection inputs is associated with selecting a final output from  
6 among output from the plurality of registers; and  
7 the step of programming the second set of selection inputs is based on the pre-  
8 selected polynomial key word.

1 4. The method as recited in Claim 1, further comprising:  
2 using a first set of multiplexers in conjunction with a first set of selection inputs for  
3 selecting at least one input for shifting data to a next shift register of the plurality  
4 of registers, wherein the at least one input is a member of a set of inputs that

5 includes an output from an adjacent logic gate and a straight shift input from an  
6 adjacent register of the plurality of registers.

1 5. The method as recited in Claim 1, further comprising:  
2 using a second set of multiplexers in conjunction with a second set of selection inputs for  
3 selecting at least one input to a corresponding logic gate, wherein the at least one  
4 input is a member of a set of inputs that includes a primary input and a feedback  
5 input.

1 6. The method as recited in Claim 1, further comprising:  
2 using a second set of multiplexers in conjunction with a second set of selection inputs for  
3 selecting a final output from among output from the plurality of registers.

1 7. The method as recited in Claim 1, wherein the plurality of registers are shift registers.

1 8. A method for generating a Cyclic Redundancy Check (CRC) generator in a system  
2 comprising the steps of:  
3 creating a circuit comprising a plurality of registers wherein each of the plurality of  
4 registers is associated with a corresponding logic gate; and  
5 programming a first set of selection inputs, wherein:  
6 the step of programming the first set of selection inputs is based on a pre-selected  
7 polynomial that is associated with the CRC generator;  
8 the first set of selection inputs is associated with:  
9 selecting corresponding input from each of the one or more logic gates;  
10 and  
11 a shift logic that is associated with the plurality of registers; and  
12 programming a second set of selection inputs, wherein:  
13 the second set of selection inputs is associated with selecting corresponding input  
14 to each logic gate;  
15 the second set of selection inputs is associated with selecting a final output from  
16 among output from the plurality of registers; and

17 the step of programming the second set of selection inputs is based on the pre-  
18 selected polynomial that is associated with the CRC generator.

1 9. The method as recited in Claim 8, further comprising:  
2 using a first set of multiplexers in conjunction with the first set of selection inputs for  
3 selecting at least one input for shifting to a next register of the plurality of  
4 registers, wherein the at least one input is a member of a set of inputs that includes  
5 an output from an adjacent logic gate and a straight shift from an adjacent register  
6 of the plurality of registers.

1 10. The method as recited in Claim 8, further comprising:  
2 using a second set of multiplexers in conjunction with the second set of selection inputs  
3 for selecting at least one input to a corresponding logic gate, wherein the at least  
4 one input is a member of a set of inputs that includes a primary input and a  
5 feedback input.

1 11. The method as recited in Claim 8, further comprising:  
2 using a second set of multiplexers in conjunction with the second set of selection inputs  
3 for selecting the final output from among output from the plurality of registers.

1 12. The method as recited in Claim 8, wherein the plurality of registers are shift registers.

1 13. A computer-readable medium carrying one or more sequences of instructions for  
2 generating a Cyclic Redundancy Check (CRC) generator in a system, which instructions, when  
3 executed by one or more processors, cause the one or more processors to carry out the steps of:  
4 creating a circuit comprising a plurality of registers wherein each of the plurality of  
5 registers is associated with a corresponding logic gate; and  
6 programming a subset of the plurality of registers to have a value of zero and  
7 programming a corresponding subset of the logic gates to have a value of zero,  
8 wherein the step of programming is based on a pre-selected polynomial key word.

1 14. A computer-readable medium carrying one or more sequences of instructions for  
2 generating a Cyclic Redundancy Check (CRC) generator in a system, which instructions,  
3 when executed by one or more processors, cause the one or more processors to carry out  
4 the steps of:

5 creating a circuit comprising a plurality of registers wherein each of the plurality of  
6 registers is associated with a corresponding logic gate; and  
7 programming a first set of selection inputs, wherein:

8 the step of programming the first set of selection inputs is based on a pre-selected  
9 polynomial that is associated with the CRC generator;

10 the first set of selection inputs is associated with:

11 selecting corresponding input from each of the one or more logic gates;  
12 and

13 a shift logic that is associated with the plurality of registers; and

14 programming a second set of selection inputs, wherein:

15 the second set of selection inputs is associated with selecting corresponding input  
16 to each logic gate;

17 the second set of selection inputs is associated with selecting a final output from  
18 among output from the plurality of registers; and

19 the step of programming the second set of selection inputs is based on the pre-selected  
20 polynomial that is associated with the CRC generator.

1 15. An apparatus for creating a Cyclic Redundancy Check (CRC) generator in a system,  
2 comprising:  
3 means for creating a circuit comprising a plurality of registers wherein each of the  
4 plurality of registers is associated with a corresponding logic gate; and  
5 means for programming a subset of the plurality of registers to have a value of zero and  
6 programming a corresponding subset of the logic gates to have a value of zero,  
7 wherein the step of programming is based on a pre-selected polynomial key word.

1 16. An apparatus for creating a Cyclic Redundancy Check (CRC) generator in a system,  
2 comprising:  
3 means for creating a circuit comprising a plurality of registers wherein each of the  
4 plurality of registers is associated with a corresponding logic gate; and  
5 means for programming a first set of selection inputs, wherein:  
6 the step of programming the first set of selection inputs is based on a pre-selected  
7 polynomial that is associated with the CRC generator;  
8 the first set of selection inputs is associated with:  
9 selecting corresponding input from each of the one or more logic gates;  
10 and  
11 a shift logic that is associated with the plurality of registers; and  
12 means for programming a second set of selection inputs, wherein:  
13 the second set of selection inputs is associated with selecting corresponding input  
14 to each logic gate;  
15 the second set of selection inputs is associated with selecting a final output from  
16 among output from the plurality of registers; and  
17 means for the step of programming the second set of selection inputs is based on the pre-  
18 selected polynomial that is associated with the CRC generator.

1 17. An apparatus for creating a Cyclic Redundancy Check (CRC) generator in a system,  
2 comprising:  
3 a processor;  
4 one or more stored sequences of instructions which, when executed by the processor,  
5 cause the processor to carry out the steps of:  
6 creating a circuit comprising a plurality of registers wherein each of the plurality  
7 of registers is associated with a corresponding logic gate; and  
8 programming a subset of the plurality of registers to have a value of zero and  
9 programming a corresponding subset of the logic gates to have a value of  
10 zero, wherein the step of programming is based on a pre-selected  
11 polynomial key word.

1 18. An apparatus for creating a Cyclic Redundancy Check (CRC) generator in a system,  
2 comprising:  
3 a processor;  
4 one or more stored sequences of instructions which, when executed by the processor,  
5 cause the processor to carry out the steps of:  
6 creating a circuit comprising a plurality of registers wherein each of the plurality  
7 of registers is associated with a corresponding logic gate; and  
8 programming a first set of selection inputs, wherein:  
9 the step of programming the first set of selection inputs is based on a pre-  
10 selected polynomial that is associated with the CRC generator;  
11 the first set of selection inputs is associated with:  
12 selecting corresponding input from each of the one or more logic  
13 gates; and  
14 a shift logic that is associated with the plurality of registers; and  
15 programming a second set of selection inputs, wherein:  
16 the second set of selection inputs is associated with selecting  
17 corresponding input to each logic gate;  
18 the second set of selection inputs is associated with selecting a final output  
19 from among output from the plurality of registers; and  
20 the step of programming the second set of selection inputs is based on the  
21 pre-selected polynomial that is associated with the CRC generator.